

**AMENDMENTS TO THE CLAIMS**

Please cancel claims 11-17 and 21, and amend claims 18-20, as shown in the following list of claims:

Claims 1-17. (Canceled)

Claim 18. (Currently Amended) A method of manufacturing a semiconductor device having stacked ~~first and second~~ semiconductor chips, comprising:

Preparing ~~a the~~ first semiconductor chip and ~~a~~ second semiconductor chips chip, the first semiconductor chip having a first area which is larger than the area of the second semiconductor chip and is free of the formation of elements which generate heat when in operation, and a second area which surrounds the first area; and

mounting the second semiconductor chip on the first semiconductor chip so as to arrange the second semiconductor chip to cover an area wholly within ~~just above~~ the first area of the first semiconductor chip.

Claim 19. (Currently Amended) The method according to claim 18, wherein a microcontroller used as a mask ROM is formed on the first area of said first semiconductor chip, and said second semiconductor chip serves a function of a flash memory.

Claim 20. (Currently Amended) The method of claim 18, wherein the first ~~semiconductor substrate~~ area is an approximately central area of the first semiconductor chip.

Claim 21. (Canceled)

Claim 22. (Previously Presented) The method of claim 18, wherein:

the first semiconductor chip has at least one first electrode formed on the periphery of the first area, at least one second electrode formed on the periphery of the second area, and a plurality of leads disposed around said first semiconductor chip;

the second semiconductor chip has at least one third electrode formed thereon; and  
the method further comprises:

connecting the first electrode of said first semiconductor chip and the third electrode of said second semiconductor chip with at least one first metal wire; and

connecting said second electrode of said first semiconductor chip and said leads with at least one second metal wire.

Claim 23. (Previously Presented) The method according to claim 22, wherein said third electrode of said second semiconductor chip is electrically connected to said second electrode of said first semiconductor chip through a transistor formed within the second area of said first semiconductor chip.

Claims 24. (Previously Presented) The method according to claim 18, further comprising:

sealing said first and second semiconductor chips, said first and second metal wires and some of said leads with an encapsulating resin.